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**UTILITY PATENT APPLICATION TRANSMITTAL**  
**(Large Entity)***(Only for new nonprovisional applications under 37 CFR 1.53(b))*Docket No.  
87552.99R272/SE-1528PD

Total Pages in this Submission

**TO THE ASSISTANT COMMISSIONER FOR PATENTS**Box Patent Application  
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

**POWER SEMICONDUCTOR DEVICE WITH HIGH AVALANCHE CAPABILITY**

and invented by:

Jifa Hao, John L. Benjamin, Randall L. Case, Jae J. Yun

If a **CONTINUATION APPLICATION**, check appropriate box and supply the requisite information:☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: \_\_\_\_\_

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Enclosed are:

**Application Elements**

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 11 pages and including the following:
  - a. ☒ Descriptive Title of the Invention
  - b. ☐ Cross References to Related Applications *(if applicable)*
  - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
  - d. ☐ Reference to Microfiche Appendix *(if applicable)*
  - e. ☒ Background of the Invention
  - f. ☒ Brief Summary of the Invention
  - g. ☒ Brief Description of the Drawings *(if drawings filed)*
  - h. ☒ Detailed Description
  - i. ☒ Claim(s) as Classified Below
  - j. ☒ Abstract of the Disclosure

# UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.  
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Total Pages in this Submission

## Application Elements (Continued)

3. ☒ Drawing(s) (when necessary as prescribed by 35 USC 113)
- a. ☐ Formal Number of Sheets \_\_\_\_\_
- b. ☒ Informal Number of Sheets 1
4. ☒ Oath or Declaration
- a. ☒ Newly executed (original or copy) ☐ Unexecuted
- b. ☐ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional application only)
- c. ☒ With Power of Attorney ☐ Without Power of Attorney
- d. ☐ DELETION OF INVENTOR(S)  
Signed statement attached deleting inventor(s) named in the prior application,  
see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference (usable if Box 4b is checked)  
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all must be included)
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy (identical to computer copy)
- c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

## Accompanying Application Parts

8. ☒ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(B) Statement (when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
- ☐ First Class ☒ Express Mail (Specify Label No.): EL407177618US

# UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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## Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. ☐ Additional Enclosures (please identify below):

## Fee Calculation and Transmittal

### CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	34	- 20 =	14	x \$18.00	\$252.00
Indep. Claims	2	- 3 =	0	x \$78.00	\$0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$690.00
OTHER FEE (specify purpose)					\$0.00
TOTAL FILING FEE					\$942.00

- ☒ A check in the amount of **\$942.00** to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **10-0223** as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of \_\_\_\_\_ as filing fee.
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- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

  
Signature

Dated: September 1, 2000

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**CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10)**Applicant(s): **Jifa Hao, et al.**

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Group Art Unit

**Unknown**Invention: **POWER SEMICONDUCTOR DEVICE WITH HIGH AVALANCHE CAPABILITY**

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Docket No.

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Examiner

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Group Art Unit

**Unknown**Invention: **POWER SEMICONDUCTOR DEVICE WITH HIGH AVALANCHE CAPABILITY**JC91B U.S. PTO  
09/654845

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**POWER SEMICONDUCTOR DEVICE  
WITH HIGH AVALANCHE CAPABILITY  
AND PROCESS FOR FORMING SAME**

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Field of the Invention

The present invention relates to semiconductor devices and, more particularly, to power devices having high avalanche capability and a process for making them.

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Background of the Invention

Many applications for power semiconductors require fast switching devices having low power dissipation. Anderson et al., U.S. Patent No. 5,119,148, the disclosure of which is incorporated herein by reference, describes a high voltage (600-1000 volts or higher), fast damper diode comprising P<sup>+</sup>, P<sup>-</sup>, N<sup>-</sup>, N<sup>+</sup> layer wherein the P<sup>-</sup> and N<sup>-</sup> layers are of substantially equal thickness, each greater than about 50 μm, and have substantially equal doping density of less than about 10<sup>15</sup> atoms/cm<sup>3</sup>. Lutz et al., U.S. Patent No. 5,747,872, the disclosure of which is incorporated herein by reference, describes a fast power diode comprising P<sup>+</sup>, N<sup>-</sup>, and N<sup>+</sup> doping zones, and recombination centers formed by electron irradiation and platinum diffusion in the N<sup>-</sup> and N<sup>+</sup> zones.

20

Among the measures of diode performance are the following: rated forward current (IF), forward voltage drop (VF), transient forward recovery time (TFR), transient turn-on peak overshoot voltage (TOPO), diode reverse blocking voltage (BVR), transient reverse recovery time (TRR), and unclamped inductive switching (UIS), which is a measure of the amount of avalanche energy that can be dissipated in the device without destructive failure.

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BVR and UIS can be increased by increasing the resistivity and/or the thickness of the diode depletion region, but this typically results in also increasing TFR and TOPO. TRR can be lowered by the introduction of recombination centers, but this also generally leads to an increase in VF. TOPO and VF may be reduced and IF increased by increasing the diode area, i.e., die size, but this is undesirable both from the view point of cost and the trend toward reducing device size.

30

Because the rapid switching of high currents can result in the generation by parasitic inductance of voltage spikes that reach the breakdown voltage of a device, there is an ongoing

need for power semiconductor devices in switching applications, for example, where the dissipation of large amounts of avalanche energy without damage is required. The present invention meets this need.

## Summary of the Invention

The present invention is directed to a power semiconductor device having high avalanche capability and comprising an  $N^+$  doped substrate and, in sequence,  $N^-$  doped,  $P^-$  doped, and  $P^+$  doped semiconductor layers, the  $P^-$  and  $P^+$  doped layers having a combined thickness of about 5  $\mu m$  to about 12  $\mu m$ . Recombination centers comprising noble metal impurities are disposed substantially in the  $N^-$  and  $P^-$  doped layers.

The present invention is further directed to a process for forming a power semiconductor device with high avalanche capability that comprises: forming an N<sup>-</sup> doped epitaxial layer on an N<sup>+</sup> doped substrate, forming a P<sup>-</sup> doped layer in the N<sup>-</sup> doped epitaxial layer, forming a P<sup>+</sup> doped layer in the P<sup>-</sup> doped layer, and forming in the P<sup>-</sup> and N<sup>-</sup> doped layers recombination centers comprising noble metal impurities. The P<sup>+</sup> and P<sup>-</sup> doped layers have a combined thickness of about 5 μm to about 12 μm.

The present invention beneficially provides devices of small die size whose UIS performance is comparable to that of conventional devices of much larger die size.

### Brief Description of the Drawings

FIG. 1 is a schematic representation of a prior art diode comprising a P<sup>+</sup> doped layer formed in an N<sup>-</sup> epitaxial layer that is disposed on an N<sup>+</sup> semiconductor substrate.

### Detailed Description of the Invention

In FIG. 1 is schematically depicted a prior art power diode 100 that includes P<sup>+</sup> doped, N<sup>-</sup> doped, and N<sup>+</sup> doped semiconductor layers 101, 102, and 103, respectively. Also included in diode 100 is a heavily N<sup>+</sup> doped source region 104 and a field oxide layer 105.

5 The arrows E indicate the electrical field at the corner of the pn junction of diode 100 in the reverse biased condition.

FIG. 2 schematically illustrates a power diode 200 in accordance with the present invention that includes P<sup>+</sup> doped, P<sup>-</sup> doped, and N<sup>-</sup> doped layers 201, 202, and 203, respectively, on an N<sup>+</sup> doped semiconductor substrate 204. Layer 203 preferably is epitaxially formed on substrate 204, which can be doped with antimony, phosphorus, or, preferably, arsenic. N<sup>-</sup> doped epitaxial layer 203 can be grown with a dopant level of about 10<sup>14</sup> atoms/cm<sup>3</sup> to about 10<sup>15</sup> atoms/cm<sup>3</sup> of arsenic or, preferably, phosphorus.

10 Layers 201 and 202 are formed by dopant implantation and/or diffusion into epitaxial layer 203. Shallow P<sup>+</sup> doped layer 201 has a thickness preferably of about 0.1 μm to about 2 μm, and P<sup>-</sup> doped layer 202 has a thickness preferably of about 4 μm to about 10 μm. P<sup>+</sup> doped layer 201 and P<sup>-</sup> doped layer 202 together have a combined thickness of about 5 μm to about 12 μm. Shallow P<sup>+</sup> doped layer 201 has a dopant level preferably of at least 10<sup>18</sup> atoms/cm<sup>3</sup>, more preferably, about 6x10<sup>19</sup> atoms/cm<sup>3</sup>. P<sup>-</sup> doped layer 202 has a dopant level preferably of at least 10<sup>16</sup> atoms/cm<sup>3</sup>, more preferably, about 2.5x 10<sup>17</sup> atoms/cm<sup>3</sup>. A preferred dopant for layers 201 and 202 is boron.

15 Recombination centers comprising noble metal impurities are introduced into N<sup>-</sup> doped layer 203 and P<sup>-</sup> doped layer 202, preferably by diffusion through N<sup>+</sup> doped substrate 204. Noble metal impurities are selected from the group consisting of gold, platinum, and palladium, platinum being preferred. Diffusion of platinum is carried out at a temperature of, preferably, about 940°C, resulting in a concentration of platinum in diode 200 of about 1x10<sup>15</sup> to about 1x10<sup>16</sup> atoms/cm<sup>3</sup>, preferably about 2 x10<sup>15</sup> atoms/cm<sup>3</sup>. Lowering the platinum diffusion temperature from 950°C to 940°C reduces the concentration of platinum impurities and improves the avalanche capability of diode 200.

20 Also included in diode 200 is a heavily N<sup>+</sup> doped source region 205, which provides a channel stop for improved reliability, and a field oxide layer 206. As shown by a comparison of FIGS. 1 and 2, the electrical field, represented by the arrows E, is substantially more



dispersed at the corner of the pn junction of diode 200 of the present invention compared with prior art diode 100.

A heavily arsenic doped  $N^+$  substrate on which is formed a phosphorus doped  $N^-$  epitaxial layer with a thickness of about 21  $\mu m$  to about 27  $\mu m$ , preferably about 25  $\mu m$ , is used to form a series of control devices and devices of the present invention. For the control device series, whose general structure is represented by FIG. 1, a heavily  $P^+$  doped layer is formed by boron implantation and diffusion to a depth of about 8-10  $\mu m$ . Prior to metallization, platinum is deposited on the bottom of the substrate and diffused at a temperature of about 950°C, resulting in a platinum concentration in the  $N^-$  layer of about  $5.8 \times 10^{15}$  atoms/cm<sup>3</sup>. The control series includes devices with die sizes of 160x160 mil<sup>2</sup> (ca. 4x 4 mm<sup>2</sup>), 80x80 mil<sup>2</sup> (ca. 2x2 mm<sup>2</sup>), and 60x60 mil<sup>2</sup> (ca. 1.5x1.5 mm<sup>2</sup>).

The epitaxial wafer used to form the series of control devices is also employed to form a series of devices in accordance with the present invention, whose general structure is represented by FIG. 2. A  $P^-$  doped layer having an average concentration of about  $2.5 \times 10^{17}$  atoms/cm<sup>3</sup> is formed by boron implantation and diffusion to a depth of about 8-10  $\mu m$ , followed by heavy boron doping to form a  $P^+$  doped layer having a concentration of about  $6 \times 10^{19}$  atoms/cm<sup>3</sup> and extending to a depth of about 1-2  $\mu m$ . Prior to metallization, platinum is deposited on the bottom of the substrate and diffused at a temperature of about 940°C, resulting in a platinum concentration in the  $N^-$  layer of about  $2.0 \times 10^{15}$  atoms/cm<sup>3</sup>. Following platinum diffusion, the devices are allowed to cool slowly to about 600°C at a rate of about 3°C/minute. As with the control series, the series formed in accordance with the present invention includes devices with die sizes of 160x160 mil<sup>2</sup> (ca. 4x 4 mm<sup>2</sup>), 80x80 mil<sup>2</sup> (ca. 2x2 mm<sup>2</sup>), and 60x60 mil<sup>2</sup> (ca. 1.5x1.5 mm<sup>2</sup>).

As noted above, unclamped inductive switching (UIS) is a measure of avalanche energy that can be dissipated in a device without causing its destructive failure. FIG. 3 schematically illustrates a standard test circuit for UIS measurement. Energy is first stored in an inductor L by turning on a switching transistor T (an IGBT or MOSFET, for example) during a period of time proportional to the peak current desired in inductor L. When transistor T is off, inductor L releases its current and avalanches a test device DUT until all the energy is transferred.

Measurements of VF, TRR, and BVR by standard procedures are made on the series of control devices and devices of the invention, and the results, each the average of measurements on about 2000-5000 devices, depending on die size, are presented in TABLE 1. Similar values of VF and BVR are obtained for all of the devices, both control and of the invention, regardless of die size. The TRR results do vary with die size but, for a given size, the TRR of the device of the invention is practically the same as the control, despite the lower level of platinum in the former, the result of a diffusion temperature 10°C lower than that employed for the control device. Using a reduced concentration of platinum to achieve low VF values without increasing TRR values is an important advantage, especially for devices having voltages on the order of 200 volts.

TABLE 1

	Die Size (mil <sup>2</sup> )	Pt Concentration (x 10 <sup>15</sup> atoms/cm <sup>3</sup> )	VF (volts)	TRR (ns)	BVR (volts)	UIS (mJ)
Control 1	160	5.8	0.900 ± 0.010	32-34	259 ± 105	<20
Sample 1	160	2.0	0.909 ± 0.098	30-32	251 ± 9.8	>304
Control 2	80	5.8	0.905 ± 0.010	19-20	259 ± 17.4	<0.8
Sample 2	80	2.0	0.893 ± 0.009	21-22	257 ± 13.1	125
Control 3	60	5.8	0.919 ± 0.010	18-19	255 ± 6.4	0
Sample 3	60	2.0	0.908 ± 0.010	19-20	264 ± 6.4	72

TABLE 1 includes the results of UIS measurements carried out on control devices and devices of the present invention. The UIS data presented show the very large improvement in avalanche capability of the devices of the invention compared with those of control devices whose measured properties are otherwise very similar. Thus, the present invention enables the substitution of a much smaller size die to achieve UIS performance comparable to that of a larger conventional die.

The present invention is also applicable to MOSFET and IGBT power devices. FIG. 4 schematically depicts a portion of a device 400 in accordance with the present invention that includes P<sup>+</sup> doped, P<sup>-</sup> doped, and N<sup>-</sup> doped semiconductor layers 401, 402, and 403, respectively, on a substrate (not shown). A heavily doped N<sup>+</sup> region 404 is adjacent P<sup>+</sup> and P<sup>-</sup> doped layers 401 and 402, respectively. Also shown is a gate oxide layer 405. The structure shown in FIG. 4 enables lateral current flow to be reduced and the breakdown region to be shifted to the active area during avalanche. In accordance with the present invention, a MOSFET further comprises an N<sup>+</sup> drain region (not shown) below N<sup>-</sup> layer 403; an IGBT includes a P<sup>+</sup> collector region (not shown) below layer 403. In the MOSFET or IGBT, the desired effect is the occurrence of avalanche breakdown at the vertical body-drain diode, without turning on the bipolar junction transistor (BJT) and causing the second breakdown.

The invention has been described in detail for the purpose of illustration, but it is to be understood that such detail is solely for that purpose, and variations can be made therein by those skilled in the art without departing from the spirit and scope of the invention, which is defined by the claims that follow.

## What Is Claimed Is:

1. A power semiconductor device having high avalanche capability, said device comprising:

an  $N^+$  doped substrate and, in sequence,  $N^-$  doped,  $P^-$  doped, and  $P^+$  doped semiconductor layers, said  $P^-$  doped and  $P^+$  doped layers having a combined thickness of about  $5\mu m$  to about  $12\mu m$ ; and

recombination centers comprising noble metal impurities disposed substantially in said  $N^-$  doped and  $P^-$  doped layers.

2. The device of claim 1 wherein said  $P^-$  doped layer has a thickness of about  $4\mu m$  to about  $10\mu m$ .

3. The device of claim 1 wherein said  $P^+$  doped layer has a thickness of about  $0.1\mu m$  to about  $2\mu m$ .

4. The device of claim 1 wherein said  $P^-$  doped layer has a dopant level of at least  $10^{16}$  atoms/cm<sup>3</sup>.

5. The device of claim 4 wherein said  $P^-$  doped layer has a dopant level of about  $2.5 \times 10^{17}$  atoms/cm<sup>3</sup>.

6. The device of claim 1 wherein said  $P^+$  doped layer has a dopant level of at least  $10^{18}$  atoms/cm<sup>3</sup>.

7. The device of claim 6 wherein said  $P^+$  doped layer has a dopant level of about  $6 \times 10^{19}$  atoms/cm<sup>3</sup>.

8. The device of claim 1 wherein said  $N^-$  doped layer has a dopant level of about  $10^{14}$  atoms/cm<sup>3</sup> to about  $10^{15}$  atoms/cm<sup>3</sup>.

9. The device of claim 1 wherein said N<sup>-</sup> doped, P<sup>-</sup> doped, and P<sup>+</sup> doped semiconductor layers are epitaxial layers.
10. The device of claim 1 wherein said noble metal impurities are selected from the group consisting of gold, platinum, and palladium.
11. The device of claim 10 wherein said noble metal impurities comprise platinum.
12. The device of claim 11 wherein said recombination centers are formed by platinum diffusion through said N<sup>+</sup> doped substrate into said N<sup>-</sup> doped and P<sup>-</sup> doped layers.
13. The device of claim 11 containing platinum impurities at a concentration of about 1x10<sup>15</sup> to about 1x10<sup>16</sup> atoms/cm<sup>3</sup>.
14. The device of claim 13 wherein said concentration of platinum impurities is about 2 x10<sup>15</sup> atoms/cm<sup>3</sup>.
15. The device of claim 1 further comprising an N<sup>+</sup> doped region disposed in said N<sup>-</sup> doped layer.
16. The device of claim 1 further comprising an N<sup>+</sup> doped region disposed adjacent said P<sup>+</sup> and P<sup>-</sup> doped layers.
17. The device of claim 16 comprising a MOSFET or an IGBT power device.
18. A process for forming a power semiconductor device having high avalanche capability, said process comprising:  
forming an N<sup>-</sup> doped epitaxial layer on an N<sup>+</sup> doped substrate;  
forming a P<sup>-</sup> doped layer in said N<sup>-</sup> doped epitaxial layer;  
forming a P<sup>+</sup> doped layer in said P<sup>-</sup> doped layer, said P<sup>+</sup> doped and P<sup>-</sup>

doped layers having a combined thickness of about 5  $\mu\text{m}$  to about 12  $\mu\text{m}$ ; and  
forming in said P<sup>-</sup> doped and N<sup>-</sup> doped layers recombination centers  
comprising noble metal impurities.

19. The process of claim 18 wherein said P<sup>-</sup> doped layer has a thickness of  
about 4  $\mu\text{m}$  to about 10  $\mu\text{m}$ .

20. The process of claim 18 wherein said P<sup>+</sup> doped layer has a thickness of  
about 0.1  $\mu\text{m}$  to about 2  $\mu\text{m}$ .

21. The process of claim 18 wherein said P<sup>-</sup> doped layer has a dopant level of at  
least  $10^{16}$  atoms/cm<sup>3</sup>.

22. The process of claim 21 wherein said P<sup>-</sup> doped layer has a dopant level of  
about  $2.5 \times 10^{17}$  atoms/cm<sup>3</sup>.

23. The process of claim 18 wherein said P<sup>+</sup> doped layer has a dopant level of at  
least  $10^{18}$  atoms/cm<sup>3</sup>.

24. The process of claim 23 wherein said P<sup>+</sup> doped layer has a dopant level of  
about  $6 \times 10^{19}$  atoms/cm<sup>3</sup>.

25. The process of claim 18 wherein said N<sup>-</sup> doped layer has a dopant level of  
about  $10^{14}$  atoms/cm<sup>3</sup> to about  $10^{15}$  atoms/cm<sup>3</sup>.

26. The process of claim 18 wherein said noble metal impurities are selected from  
the group consisting of gold, platinum, and palladium.

27. The process of claim 26 wherein said noble metal impurities comprise  
platinum.

28. The process of claim 27 wherein said forming said recombination centers comprises diffusing platinum through said N<sup>+</sup> doped substrate into said N<sup>-</sup> and P<sup>-</sup> doped layers.

29. The process of claim 28 platinum impurities are present in said N<sup>-</sup> and P<sup>-</sup> doped layers at a concentration of about  $1 \times 10^{15}$  to about  $1 \times 10^{16}$  atoms/cm<sup>3</sup>.

30. The process of claim 29 wherein said concentration of platinum impurities is about  $2 \times 10^{15}$  atoms/cm<sup>3</sup>.

31. The process of claim 28 wherein said diffusing is carried out at a temperature of about 940°C.

32. The process of claim 31 further comprises cooling said device to a temperature of about 600°C at a rate of about 3°C/minute.

33. The process of claim 18 further comprising forming an N<sup>+</sup> doped region in said N<sup>-</sup> doped layer.

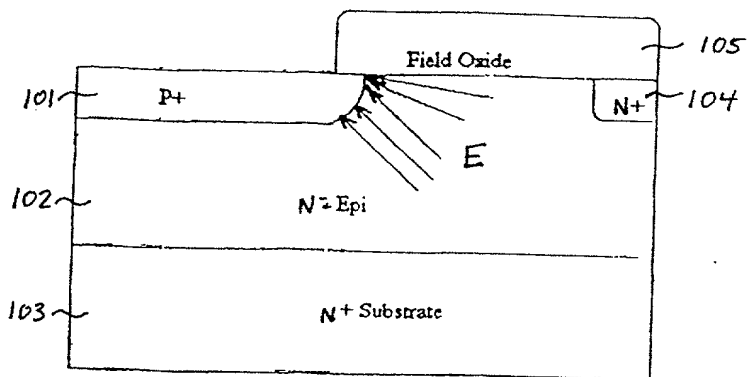
34. The process of claim 18 further comprising forming an N<sup>+</sup> doped region in said P<sup>-</sup> doped layer adjacent said P<sup>+</sup> doped layer.

### Abstract of the Disclosure

A power semiconductor device having high avalanche capability comprises an  $N^+$  doped substrate and, in sequence,  $N^-$  doped,  $P^-$  doped, and  $P^+$  doped semiconductor layers, the  $P^-$  and  $P^+$  doped layers having a combined thickness of about  $5\text{ }\mu\text{m}$  to about  $12\text{ }\mu\text{m}$ .

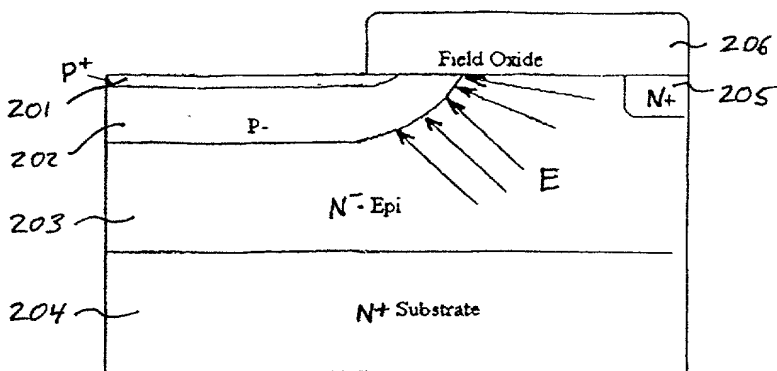
5 Recombination centers comprising noble metal impurities are disposed substantially in the  $N^-$  and  $P^-$  doped layers. A process for forming a power semiconductor device with high avalanche capability comprises: forming an  $N^-$  doped epitaxial layer on an  $N^+$  doped substrate, forming a  $P^-$  doped layer in the  $N^-$  doped epitaxial layer, forming a  $P^+$  doped layer in the  $P^-$  doped layer, and forming in the  $P^-$  and  $N^-$  doped layers recombination centers  
10 comprising noble metal impurities. The  $P^+$  and  $P^-$  doped layers have a combined thickness of about  $5\text{ }\mu\text{m}$  to about  $12\text{ }\mu\text{m}$ .





100

FIG. 1 (PRIOR ART)



200

FIG. 2

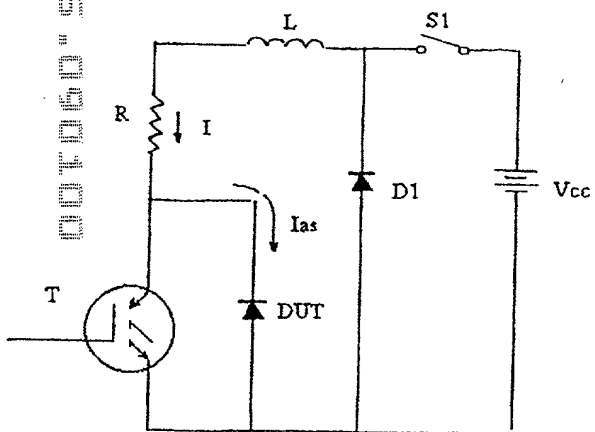
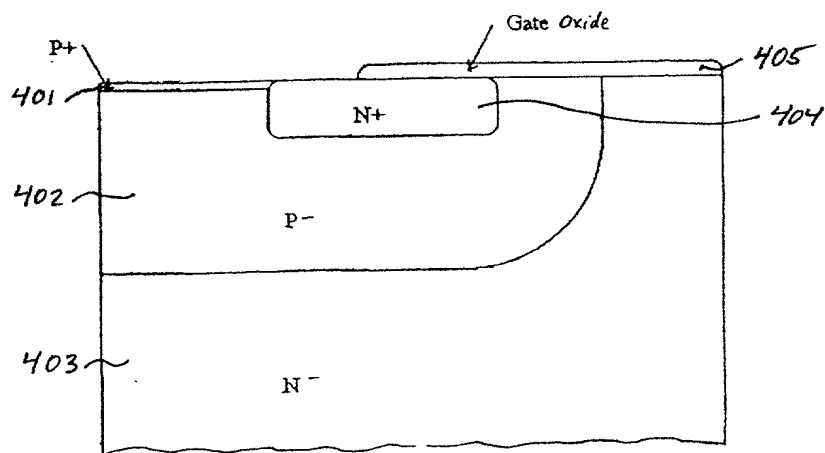


FIG. 3



400

FIG. 4

001060" 54245360

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**DECLARATION FOR UTILITY OR  
DESIGN  
PATENT APPLICATION  
(37 CFR 1.63)**

☒ Declaration Submitted with Initial Filing      OR      ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number      87552.99R272/SE-1528PD

First Named Inventor      Jifa Hao, et al.

**COMPLETE IF KNOWN**

Application Number      TBA

Filing Date      Herewith

Group Art Unit      Unknown

Examiner Name      Unknown

As a below named inventor, I hereby declare

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

POWER SEMICONDUCTOR DEVICE WITH HIGH AVALANCHE CAPABILITY

☒ the specification of which      (Title of the Invention)

is attached hereto

OR

☐ was filed on (MM/DD/YYYY)

as United States Application Number or PCT International

Application Number      TBA      and was amended on (MM/DD/YYYY)      (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
None			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below

Application Number(s)	Filing Date (MM/DD/YYYY)	<input type="checkbox"/> Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.
None		

[Page 1 of 2]

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO:

Please type a plus sign (+) inside this box → ☐

PTO/SB/01 (12-97)  
Approved for use through 9/30/00 OMB 0651-0032  
Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

## DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)
None		

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

☐ Customer Number

OR

☒ Registered practitioner(s) name/registration number listed below

Place Customer  
Number Bar Code  
Label here

Name	Registration Number	Name	Registration Number
Thomas R. FitzGerald	26,730	Ronald S. Kareken	20,573
Lee J. Fleckenstein	36,136	Laurence S. Roach	45,044
Ronald J. Kisicki	38,205	Douglas A. Balog	42,288
Bidyut K. Niyogi	27,071		

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to:

☐ Customer Number or  
Bar Code Label

OR ☒ Correspondence address below

Name	Thomas R. FitzGerald				
Address	Jaackle Fleischmann & Muegel, LLP				
Address	39 State Street				
City	Rochester	State	NY	ZIP	14614-1310
Country	USA	Telephone	(716) 262-3640	Fax	(716) 262-4133

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor:	<input type="checkbox"/> A petition has been filed for this unsigned inventor						
Given Name (first and middle (if any))			Family Name or Surname				
Jifa			Hao				
Inventor's Signature					Date	8/21/2000	
Residence: City	White Haven	State	PA	Country	USA	Citizenship	CHINA
Post Office Address	300 Elmira Street, #4						
Post Office Address							
City	White	State	PA	ZIP	18661	Country	USA

☒ Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.

Please type a plus sign (+) inside this box → +

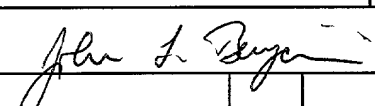
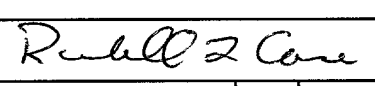
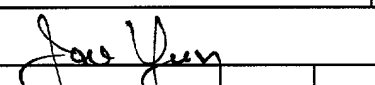
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## DECLARATION

ADDITIONAL INVENTOR(S)  
Supplemental Sheet  
Page 1 of 1

<b>Name of Additional Joint Inventor, if any:</b>				<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name (first and middle [if any])				Family Name or Surname			
John L.				Benjamin			
Inventor's Signature				Date		8/21/03	
Residence: City	Mountaintop	State	PA	Country	USA	Citizenship	USA
Post Office Address	185 Sutherland Drive						
Post Office Address							
City	Mountaintop	State	PA	ZIP	18707	Country	USA
<b>Name of Additional Joint Inventor, if any:</b>				<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name (first and middle [if any])				Family Name or Surname			
Randall L.				Case			
Inventor's Signature				Date		8/25/00	
Residence: City	Mountaintop	State	PA	Country	USA	Citizenship	USA
Post Office Address	3650 Blytheburn Road						
Post Office Address							
City	Mountaintop	State	PA	ZIP	18707	Country	USA
<b>Name of Additional Joint Inventor, if any:</b>				<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name (first and middle [if any])				Family Name or Surname			
Jae J.				Yun			
Inventor's Signature				Date		8/22/2000	
Residence: City	Mountaintop	State	PA	Country	USA	Citizenship	USA
Post Office Address	297 Schultz Lane						
Post Office Address							
City	Mountaintop	State	PA	ZIP	18707	Country	USA

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09 SEP 2003 10:50 AM



**INTERSIL CORPORATION**  
**Assignment**

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As a below named inventor or joint inventor of an invention or improvement entitled:

**POWER SEMICONDUCTOR DEVICE WITH HIGH AVALANCHE  
CAPABILITY**

for which I have executed an application for Letters Patent of the United States of America, on an even date herewith; and

WHEREAS, INTERSIL CORPORATION, a corporation organized and existing under the laws of the State of Delaware, having its principal office and place of business in the City of Palm Bay, State of Florida, is desirous of obtaining the entire right, title and interest in, to and under the said invention and the said application in the United States of America and in any and all countries foreign thereto;

NOW THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, I have sold, assigned, transferred, and set over, and by these presents do hereby sell, assign, transfer and set over, unto said INTERSIL CORPORATION, its successors, legal representatives, and assigns, my entire right, title and interest in, to, and under the said invention, and the said application, and all divisional, renewal, substitutional, and continuation applications thereof, and all Letters Patent of the United States of America which may be granted thereof and all reissues and extensions hereof, and all applications for Letters Patents which may be filed for said invention in any country or countries foreign to the United States of America, including all rights of priority, all rights to publish cautionary notices reserving ownership of said invention, all rights to register said invention in appropriate registries, and all Letters Patent which may be granted for said invention in any country or countries foreign to the United States of America, and all extensions, renewals, and reissues thereof, and I hereby authorize and request the Commissioner of Patents and Trademarks of the United States of America, and any official of any country or countries foreign to the United States of America, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said invention to said INTERSIL CORPORATION, its successors, legal representatives, and assigns, in accordance with the terms of this instrument.

And I hereby covenant that I have full right to convey the entire interest herein assigned, and that I have not executed, and will not execute, any agreement in conflict herewith.

And I hereby further covenant and agree that I will communicate to said INTERSIL CORPORATION, its successors, legal representatives, and assigns, any fact known to me respecting said invention, and testify in any legal proceeding, sign all lawful papers, execute all divisions, renewal, substitutional, continuing, and reissue applications, make all rightful declarations and/or oaths and generally do everything possible to aid said INTERSIL CORPORATION, its successors, legal representatives, and assigns, to obtain and enforce proper patent protection for said invention in all countries.

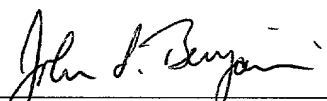
007060 " 54945960

IN TESTIMONY WHEREOF, I authorize and affirm said assignments with the signatures set forth below on the indicated date(s).

Inventor:

  
\_\_\_\_\_  
Jifa Hao

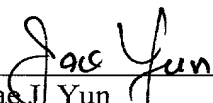
Date: 8/21, 2000

  
\_\_\_\_\_  
John L. Benjamin

Date: 8/21, 2000

  
\_\_\_\_\_  
Randall L. Case

Date: 8/25, 2000

  
\_\_\_\_\_  
Jae J. Yun

Date: 8/22, 2000